Note ATL-AL-LAL-ES-1.0

Format for the Data read out from the front-end boards

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1 General characteristics of the front-end boards

- 8 calorimeter cells correspond to an ADC on the front end board.
- The data from each ADC plus some control words are written into a Fifo, 16 bits wide
- There are five types of Fifo words : Data, Read Address, Control, Start Event Transfer, End Event Transfer.
- The Read Address, Control, Start Event Transfer and End Event Transfer words are put into the Fifo, such that the data in the Fifo is already formatted and ready to be sent out.
- At the output of the Fifo, each of the two bytes is serialised : a 16 bit Fifo word is therefore transmitted on only two lines, at 40 MHz.
- The msb is sent first and the lsb is sent last.
- Just before the output connector of the front-end board, we find a 32 bit register, receiving synchronously the 16 groups of 2 signals (one group per Fifo).
- On the output connector, we find the 32 signals from the register and a single 40 MHz clock which never stops, to strobe them.
- In a run, the number of words per event is always the same, and the same in each Fifo. The Read Address, Control and Data words always appear at the same position for each event.

- All words between a Start Event Transfer and an End Event Transfer correspond to the event being transferred and are meaningful. The time delay between Start Event Transfer and End Event Transfer is the same for all links, for all events in a Run.
- The two words following a Start Event Transfer are Control words numbers 1 and 2. The word just before an End Event Transfer is Control Word number 3.
- For each of the FIFOs,
  - all 16 bits at 1 means Start Event Transfer
  - all 16 bits at 0 means End Event Transfer
  - bit 15 is 0 for all words except Start Event Transfer
  - bit 14 is the "odd parity" of the word (e.g. 1 if all other bits are 0), except Start Event Transfer and End Event Transfer
  - bits 12 and 13 are both at 0 for all words except Data words and Start Event Transfer
- Words are continuously extracted from each Fifo at 5 MHz (5 MHz $\times$ 8 bits = 40 MHz). When the Fifo is empty, the extracted word should be 0 (i.e. same as an End Event Transfer word).
- The word rate of 5 MHz allows 50 words per event in each Fifo with an event rate as high as 100 kHz.
- The total bandwidth out of the front end board is 1.28 GBit/s.
- At least two words separate the last significant word in an event from the first significant word in the next event : the End Event Transfer and the next Start Event Transfer. This represents 400 ns.

2 Data Format in a Fifo

The detailed format of the data in a Fifo is not yet fixed. A possibility is (in the case of 5 samples per event) :

1) Start Event Transfer (all bits at 1)
2) Control word number 1
3) Control word number 2
4) Read Address (sample 1)
5) Data (Channel 1, sample 1)
6) Data (Channel 2, sample 1)
.....
12) Data (Channel 8, sample 1)
13) Read Address (sample 2)
14) Data (Channel 1, sample 2)
......

21) Data (Channel 8, sample 2)
22) Read Address (sample 3)
......
31) Read Address (sample 4)
....
40) Read Address (sample 5)
......
49) Control word number 3
50) End Event Transfer (all bits at 0)

• *The samples are not sent in chronological order. The order depends on the way the gain is chosen, which is described elsewhere. In the following, sample i is the ith sample sent by the FEB to the ROD. One possibility is sample 1 is indeed the third sample (corresponding to the maximum of the signal) is sent first, samples 2 and 3 being indeed the first and second samples. Samples 4 and 5 would be the fourth and fifth samples.*

• *If the number of samples is greater than 5, the 48 first words are the same as above, and the other samples are after. If we have 2, 3 or 4 samples, then the first sample read might be sample 2.*

• *In normal conditions, the number of words in each Fifo is* $N_W = 5 + 9 \times N_S$, *where* N_S *is the number of samples per event (between 1 and 32, 5 in normal conditions). It might be more if several gains are systematically digitized (special test runs).*

3 Case of samples common to two events

The first event is completely normal. The second event has the same number of words as normal. The fact that it follows closely the previous trigger is signalled in bits 10 and 11 of control word number 1. The order of the samples is the same as usual (third sample first, then first and second samples...). The samples which are common, and have already been sent as part of the previous event, are replaced by "dummy samples", obtained by reading the SCA at the correct read address **again**.

4 Format of each word

4.1 Format of a 16 bit Data word

bits 0-11 : ADC
bits 12-13 : Gain (11 = high gain, 10 = medium gain, 01 = low gain)
bit 14 : odd parity
bit 15 : 0

bits 12 and 13 both at 0 is forbidden. This gain coding scheme has been chosen for the SCA chip

4.2 Format of a 16 bit Read Address word

bits 0-7 : Address
bits 8-11: ADC number
bit 12 : 0
bit 13 : 0
bit 14 : odd parity
bit 15 : 0

The ADC number might be replaced by the sample number

4.3 Format of a 16 bit Control word

Control word number 1 :
bits 0-4 : Front-end board number (in the crate)
bits 5-8 : Configuration version (see below)
bit 9 : 1 if previous trigger less than N_{ov} clock cycles before current one ($N_{ov} = 16$)
bit 10 : 1 if previous trigger is N_1 clock cycles before current one ($N_1 = 3$)
bit 11 : 1 if previous trigger is N_2 clock cycles before current one ($N_2 = 4$)
bit 12 : 0
bit 13 : 0
bit 14 : odd parity
bit 15 : 0

Control word number 2 :
bits 0-11 : Bunch crossing number
bit 12 : 0
bit 13 : 0
bit 14 : odd parity
bit 15 : 0

Control word number 3 :
bit 0 : 1
bits 1-11 : Error/Status word
bit 12 : 0
bit 13 : 0
bit 14 : odd parity
bit 15 : 0

• *we can pre-define up to 16 configurations for the FEBs. For some of them, we might have the ADC number in the read address word, and we might have the Sample number for some other configurations. These bits are also used to signal special data taking conditions, such as the systematic digitization of all gains.*
• *The bunch crossing number is the real one of the event, and not simply the value of the bunch crossing counter when the trigger signal was received on the front end board.*
• *Bit 9 in Control word number 1 signals that the present signals overlap with the previous ones (i.e. the previous trigger was less than 400 ns before the current one).*
• *Bit 10 in Control word number 1 is 1 if the samples 4 to N_S of the previous event are also the samples 1 to N_S-3 of the current event (i.e. previous trigger is 75 ns before current one), and 0 otherwise.*

• *Bit 11 in Control word number 1 is 1 if the samples 5 to N_S of the previous event are also the samples 1 to N_S-4 of the current event (i.e. previous trigger is 100 ns before current one), and 0 otherwise.*
• *When Control word number 3 is read from the FIFO, it might be possible to set bit 11 to 0 if it is the last significant word of the FIFO, and to 1 otherwise.*
• *If we have two kinds of level 1 trigger signals, we have to use one bit in the event header to pass this information. In the same spirit, if we have to indicate to the ROD that a given event deserves "non-standard" processing, such as a copy into a spy memory for further monitoring, the information may be passed by the FEB, using bits 7 and 8. However, this is not envisaged at the moment.*

Word	Data Bits															
Type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BEVT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CTL1	0	P	0	0	Control bits					FEB number						
CTL2	0	P	0	0	Bunch crossing number											
RADD	0	P	0	0	ADC number				Capacitor number							
DATA	0	P	Gain		ADC Word											
CTL3	0	P	0	0	Error/status word											1
EEVT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1: Bit structure of the data word transfer from FEB to ROD.