FAST SIGNALS DISTRIBUTION FOR MODULE 0

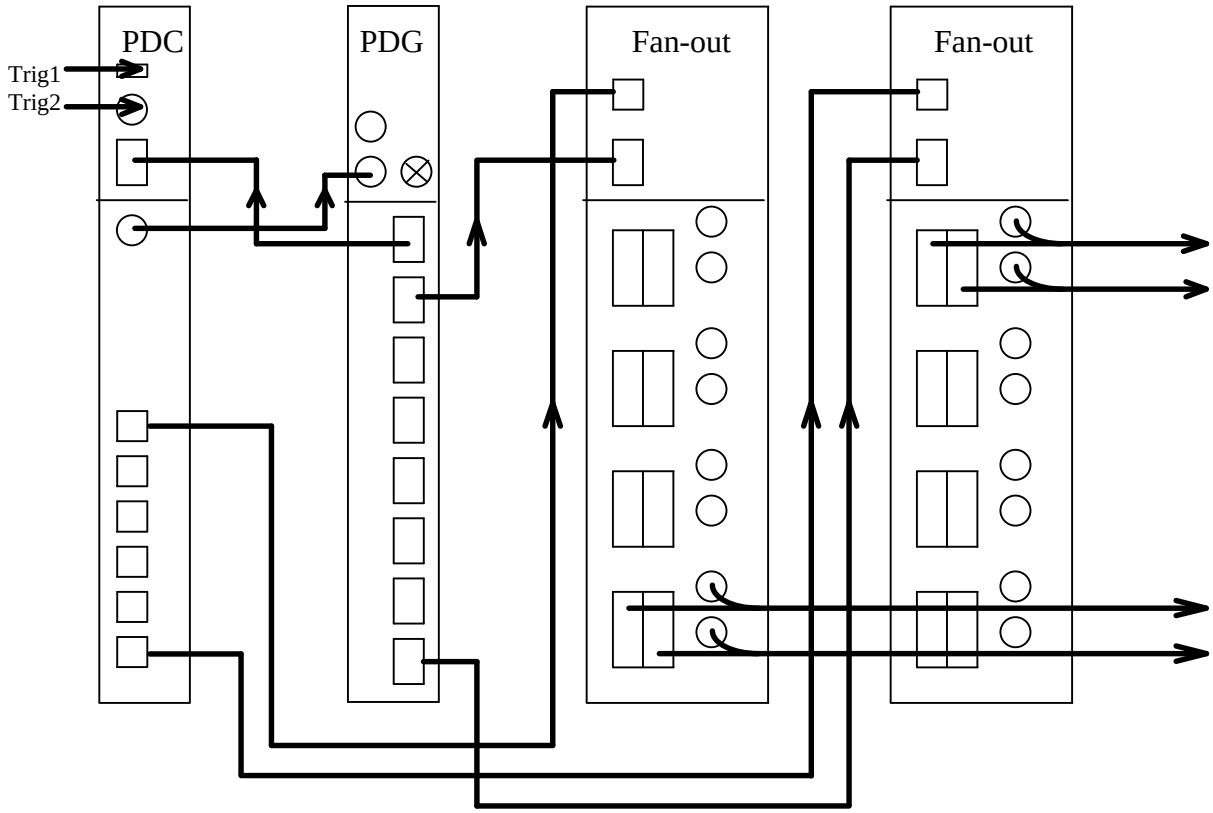
SYSTEM SPECIFICATIONS

DRAFT

Written by : R. Bernard and J. F. Renardy
To be checked by : FEB Nevis : J. Parsons, A. Gara
FEB Orsay : E. Auge
Calibration : I. Wingerter
ROD : X. Riccadonna
Beam-test : P. Fassnacht
HEC : H. Oberlack, J. Fent
To be approved by the Electronic Conveners

Introduction

This system was designed to provide the fast signals needed for the tests of the Liquid Argon Calorimeter in the CERN beams. It has also to provide these fast signals to the test benches in the laboratories responsible for the construction of the front-end electronics. This is obtained by using a modular system built out of a few VME modules. Each system is composed of one **PDG** module, one **PDC** module and up to seven **Fan-out** modules. Depending on the needs, one can get the smallest configuration with 8 outputs composed of three modules in four slots, or the largest one with 56 outputs and nine modules in 16 slots. A typical configuration is shown in the figure below; one can see the modules' interconnections, two inputs to the system (the **Trig1** and **Trig2** signals) and some **Fan-out** modules' output towards the front-end cards.



The system outputs are designed to be compatible with the inputs needed by the front-end cards : the FEB, the calibration board and the mini-ROD. Each output is conform to the specifications for the fast signals defined in the Nevis workshop ; it is composed of a bundle of the following five signals :

CLK, the main LHC clock.

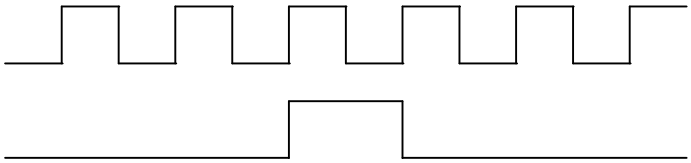
L1accept, the pulse identifying each beam crossing containing an event to be sent to the level2 trigger.

BCR, the pulse resetting the bunch counter. Occurring every 3564 cycles of the main clock.

Init, the pulse for the synchronous reset of the front-end electronics. This pulse is always accompanied by a **BCR** pulse.

Calib, the test pulse command.

The timing of each output is programmable through VME. For each output the final delay is the sum of several individual delays. The precise description of all these delays is given in the VME section. The delay applies to all the signals in the bundle, except to the Calib signal which has a special treatment. The three pulses (**L1accept, BCR** and **Init**) are exactly one cycle of the clock with the phase shown below:



Conversely, the **Calib** signal is not related to the clock.

The cables between the system output and the front-end cards are shielded. To avoid ground loops, the shields are connected to the module ground through a capacitor. It is possible to shunt this capacitor with a strap.

The inputs to the system are three connectors (two NIM and one ECL) and the VME. One NIM connector is foreseen to be used for an external clock, if one do not want to use the internal one. The two other input connectors (the **Trig1** and **Trig2** signals) can be programmed to be either an external trigger or an external calibration request. The VME commands are used to set the various delays, to perform configuration and initializations and to produce the **Init** signal and eventually some calibration sequences.

The system should be housed in a VME crate following the CERN specification V-430. Some VME master should be provided to configure and operate the system. All the modules are A32,D32 slaves and share a 4K address space at the bottom of a 16M segment.

For the use of the system in a test beam where the ATLAS LAr grounding rules apply, it is foreseen to place the VME crate in the cryostat ground. This implies that all the external connections to this crate should be galvanically isolated. The power supply should come from the cryostat mains. The trigger inputs should be isolated. The outputs to the mini-RODs should also be isolated. As the isolation requirement prevents the use of a VIC as a VME master, one should use a processor with a thin Ethernet connection to the counting room (thin Ethernet is galvanically isolated by transformer).

System description

Each system is composed of one **PDC** module, one **PDG** module and an adequate number of **Fan-out** modules. The **PDC** (programmable delay for calibration) module generates the **Calib**, **L1accept** and **Init** signals. The **PDG** (programmable delay generator) module generates the **CLK** and **BCR** signals. The **Fan-out** modules distribute these signals to the front-end cards. Each **Fan-out** module provides eight outputs. A system can contain up to seven **Fan-out** modules.

Cables and Connectors

In this system one uses three electrical signal levels :

The ECL standard (high level=-0.8V, low level=-1.6V) for one external trigger input and for many internal connections.

The PECL standard (high level=4.2V, low level=3.4V) for the transmission between this system and the front-end cards.

The NIM standard (high level=-0.8V, low level=0V) for one external trigger, the external clock and one internal connection..

By definition, a signal has a rising edge if it is going from a low level to a high level. For ECL and PECL signals, the standard IEC-192 prescribes that the reference edge of clocks and the leading edge of isolated pulses must be rising on odd pins and falling on even pins. For NIM signals, the reference edge of a clock and the leading edge of an isolated pulse must be rising. The receivers should properly terminate the circuits by using a scheme derived from standard IEC-912 for ECL and PECL signals and a 50Ω termination for NIM signals.

For the connections between modules in the crate, one uses ECL bundles and NIM signals. The NIM cables are coaxial cables with Lemo 00 connectors. The ECL cables are bundles of two (**Calib** and **Init** signal) or three (**CLK**, **L1accept** and **BCR** signal) pairs with Berg DUBOX connectors.

For the connections between the system and the front-end cards, one uses PECL bundles with special connectors : The **CLK** signal is on a bipolar Lemo 00 connector (plug FGG-

00-302-CLA35 and socket EGG-00-302-CLL or EPG-00-302-NNN). The reference edge of the clock is rising on pin 1 and falling on pin 2. The cable shield is connected through the shroud of the connector and should be connected to the receiver ground through a capacitor. The four pulse signals (**Calib**, **L1accept, BCR** and **Init**) are on a 10 pins HE 10 connector with a female plug and a male socket on the receiver card. The cable shield is connected to pins 1 and 2, and should be connected to the receiver ground through a capacitor. The signals **BCR**, **L1accept**, **Init** and **Calib** are on pins 3 through 10 in this order, as shown on the drawing above .

The PDC module.

The **PDC** module has two functions : generating the calibration sequences (see below) and implementing the larger fraction of the **L1accept** delay. This delay can be programmed, by steeps of one clock period up to 256 cycles (i.e. 6.5 μs). This delay applies equally for the calibration triggers and for the external ones. The **PDC** module can also produce the **Init** signal upon a VME command.

The **PDC** module has three inputs : two inputs for external trigger and an ECL input bundle. The external trigger inputs are the **Trig1** input accepting ECL levels and the **Trig2**

input with NIM levels. Both can be used to enter either physical triggers or calibration sequence requests, this choice being programmable through VME (see below). The ECL input bundle (**CLK**, **L1accept** and **BCR** signal) should be connected to a **PDG** output, the **L1accept** signal from the **PDG** module is not used, but is included for cable uniformity.

The **PDC** module has two kinds of outputs : the NIM trigger output to the **PDG** module and the six ECL output bundles (**Calib** and **Init** signal) to feed the **Fan-out** modules. The trigger output contains the **L1accept** for the system and should be connected to the trigger input of the **PDG** module. This trigger output is the OR of the calibration triggers and of the enabled, re-synchronized and masked external triggers. The external triggers are re-synchronized to the **PDC** clock (received from the **PDG** module) because the **L1accept** signal must be in phase with the 40MHz clock. This introduce an unavoidable jitters of ±12.5ns with respect to the external triggers. External triggers are masked to ensure that the **L1accept** signal has at least 2 untriggered cycles between **L1accept** pulses. This is done first by vetoing the external trigger inputs for 2 cycles after each **L1accept** pulse. This is also done by vetoing the external trigger inputs for a few cycles before and after each calibration trigger.

The six output bundles to the **Fan-out** modules are identical and can be used interchangeably. The **Calib** and **Init** output are long pulses (the **Init** signal is 450 ns and the **Calib** signal is programmable from 400 ns to 6.5 μs). The **Init** signal is processed by the **Fan-out** module : this signal at the output of the **PDC** module is different from the final one. All the outputs of the **PDC** module follows our synchronization rules : signal' s edges are synchronous with the reference edge of the **PDC** clock.

The PDG module

The **PDG** module provides most of the adjustable delay and also a first level of fan-out. The **PDG** module has eight outputs, but one of these must be used for the clock to the **PDC** module, leaving a maximum of seven **Fan-out** modules. The **PDC** module has only six outputs to the **Fan-out** modules, but the mini-RODs do not need the **Calib** and **Init** signal.

The **PDG** module has three NIM inputs : external clock, external trigger and external **BCR**. These inputs can be used or replaced with internal signals by suitable VME command. In this system, the **PDG** module should be configured as follow :

One should use the external trigger (from the **PDC** module).

One should not use the external **BCR** (the operation of the **PDC** module is critically dependent on the period of **BCR**).

One can use an external clock instead of the 40.08 MHz internal one.

The **PDG** module has eight ECL output bundles (**CLK**, **L1accept** and **BCR** signal). Each one can be independently delayed with a VME command. The delay can be up to 200 ns by steeps of 50 ps. In each bundle, all the signals follow our synchronization conventions.

Important notice : The external triggers are re-synchronized to the non delayed clock at the input of the **PDG** module. This does not introduce jitters because the **PDC** output is already synchronized. This can possibly produce metastable outputs when the delay of the **PDG** channel feeding the **PDC** module is set to a critical value. The actual values producing this effect depend on cable length and propagation delay and span about 150 ps every 25 ns. As these values cannot be easily predicted, typical values will be measured on the first prototype system. These critical values should be avoided.

The Fan-out module

The **Fan-out** module is basically an eight fold fan-out for the bundle of fast signals needed by the front-end cards. It also provides a small delay adjustment independently on each output bundle. Each **Fan-out** module receives part of its inputs from one output of the **PDG** module. This implies that the eight outputs of a single **Fan-out** module have the same delay ±10ns. The maximum difference in timing between two output bundles (from two different **Fan-out** modules) is 220ns.

The **Fan-out** module has two input bundles : one ECL input bundle (**Calib** and **Init** signal) from the **PDC** module and another ECL input bundle (**CLK**, **L1accept** and **BCR** signal) from the **PDG** module.

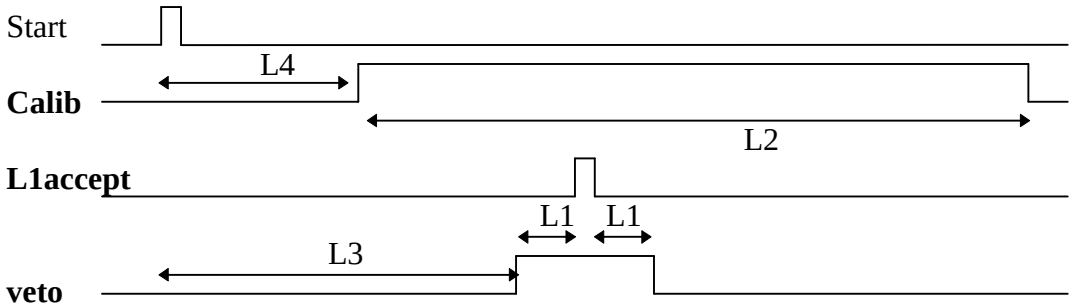
The **Fan-out** module outputs are eight PECL bundles (**CLK, Calib**, **L1accept, BCR** and **Init**). The three pulse signals (**L1accept, BCR** and **Init**) follow our synchronization rules with respect to the **CLK** signal. As the **Calib** signal is coming from the **PDC** module and is not modified by the **Fan-out** module, it is not synchronized to the **CLK** signal. Each bundle can be delayed independently with a VME command between 0 ns and 20 ns in 8 steeps of 2.5 ns.

Important notice : with the above conventions, using the **CLK** signal to sample **L1accept, BCR** or **Init** will automatically produce metastable outputs. One should either accept the synchronized signals as they are or use ~~**CLK**~~ for re-synchronization.

The Calibration Sequence

A calibration sequence is started either by a VME command (see below) or by an external signal to the **PDC** module when enabled. A calibration sequence produces a **Calib** signal, an **L1accept** pulse and a **veto** signal used to inhibit the external triggers close to the generated calibration trigger.

Inside the **PDC** module, the **Calib, L1accept** and **veto** signals have the following timing relations to the start of the calibration sequence. The four delays (L1 to L4) are described in the VME section. At the output of the **PDC** module, the **L1accept** signal is delayed by the large common delay with respect to the generated one.



At the output of the **PDC** module all these signals are synchronized to the **PDC** clock. At the output of the **Fan-out** modules, **L1accept** will still be synchronized to **CLK**, but **Calib**, which is not delayed, will no longer be synchronized.

VME Commands

All the parameters in the modules of the system are accessible from VME. Each VME register can be read and written. When reading, the value obtained is either the value set by the last write or the power-up value. The only exceptions to this rule are the two trigger bits in the **PDC** module which are erased once the trigger request has been obeyed. All registers are preset at power-up time, normally with a 0 value, except mainly the **PDG** module where a power-up configuration can be selected with a thumb wheel on the front panel.

All the modules in the system are A32,D32 slaves. They respond to the following address modifiers :

0E -- Extended Supervisor Program Access.
0D -- Extended Supervisor Data Access.
0A -- Extended Non privileged Program Access.
09 -- Extended Non privileged Data Access.

To save addressing space, all the modules in the system can be set-up in close locations as shown in the following diagram. Here XX represent the value (from 00 to FF) on the two rotary switches in each module. For the **Fan-out** module there is a third switch represented by Y and used to represent the **Fan-out** number (from 1 to 7). The symbol z represents an intermediate address (4,8 or C).

PDC	X	X	0	0	0	8	0	8
	X	X	0	0	0	8	0	4
	X	X	0	0	0	8	0	0
	X	X	0	0	0	Y	1	0
Fan-out	X	X	0	0	0	Y	0	z
	X	X	0	0	0	Y	0	0
	X	X	0	0	0	0	1	0
PDG	X	X	0	0	0	0	0	z
	X	X	0	0	0	0	0	0

VME map of the PDG module.

	31 ... 27			19	15	11 ...
ad 00	not used			MUX	not used	DLY #1
ad 04	not used	DLY #2			not used	DLY #3
ad 08	not used	DLY #4			not used	DLY #5
ad 0C	not used	DLY #6			not used	DLY #7
ad 10	not used	DLY #8			not used	

The MUX field represents the status of the NIM inputs with the following coding :

xx00 Internal trigger @ 100Hz
xx01 Internal trigger @ 100KHz
xx11 External trigger
x0xx Internal BCR
x1xx External BCR
0xxx Internal clock @ 40,08MHz
1xxx External clock

The DLY fields specify the delays in the corresponding output bundles (DLY#1 for output #1 ... DLY#8 for output #8). This delay is coded on 12 bits, the lower one representing 50 ps. The maximum delay (DLY=4095) is about 200 ns.

VME map of the Fan-out module

	31	23	18	15	2
ad 00	not used	encal		not used	DLY #1
ad 04	not used		DLY #2	not used	DLY #3
ad 08	not used		DLY #4	not used	DLY #5
ad 0C	not used		DLY #6	not used	DLY #7
ad 10	not used		DLY #8	not used	

The encal field contains the enable bits for the Calib signals. There is one bit for each channel (bit 16 is the enable for channel #1 ... bit 23 is the enable for channel #8). When the bit is ON, the Calib signal is transmitted, When the bit is OFF, the Calib signal is not transmitted.

The DLY fields specify the delays in the corresponding output bundles (DLY#1 for output #1 ... DLY#8 for output #8). This delay is coded on 3 bits, the lower one representing 2.5 ns. The maximum delay (DLY=7) is about 20 ns.

VME map of the PDC module.

	31	23	21	19	15	7	5
ad 00	Trig	not	used	Mode	not used	DLY	
ad 04	not used			L1	not used	L2	
ad 08	not used			L3	not used		L4

The Trig field contains two bits :

Bit 24 is used to trigger a calibration sequence from VME.
Bit 28 is used to trigger a **Init** pulse from VME.

These bits can be set from the VME but they are erased when the trigger is obeyed. They can be read as 1 but only during a few μs.

The Mode field controls the use of the external trigger inputs. There are two fields of two bits. Mode1 (bits 16 and 17) controls the use of the **Trig1** input, while Mode2 (bits 18 and 19) controls the use of the **Trig2** input. The coding of Mode1 and Mode2 is :

00 Trig input not used.
01 Trig input used to generate the **L1accept** signal.
11 Trig input used to start a calibration sequence.

If both Mode fields contain 01, then **L1accept** will be the OR of the two inputs with a common veto to avoid triggers not separated by 75 ns. The calibration request is the OR of the VME command (bit 00<24>) and of the trig inputs with a Mode field set to 11.

The DLY field specifies the large delay for the **L1accept** signal. This delay is coded on 8 bits, the lower one representing 25 ns. The maximum delay (DLY=255) is about 6.5 μs.

The L1 field specifies the width of the veto for external **L1accept** input. During this veto period around the **L1accept** for calibration, the external trigger inputs are disabled. This width is coded on 4 bits, the lower one representing 25 ns on both sides of the **L1accept** for calibration. The maximum total veto width (L1=15) is about 800 ns.

The L2 field specifies the width for the **Calib** signal. This width is coded on 8 bits, the lower one representing 400 ns. The maximum delay (L2=255) is about 100 μs.

The L3 field specifies the delay before the veto. The **L1accept** for calibration is generated exactly at the middle of the veto. This delay is coded on 6 bits, the lower one representing 25 ns. The maximum delay (L3=63) is about 1.4 μs.

The L4 field specifies the delay before the **Calib** signal. This delay is coded on 6 bits, the lower one representing 25 ns. The maximum delay (L4=63) is about 1.4 μs.

Computation of the Calibration Delay

At the output of the **Fan-out** module, the delay between the **Calib** signal and the **L1accept** for this calibration is the sum of the following components :

1- The programmed delay in the **PDC** module.
2- The large delay (DLY) suffered by **L1accept** in the **PDC** module.
3- The re-synchronization delay of **L1accept** at the input of the **PDG** module.
4- The variable delay in the **PDG** and **Fan-out** modules.
5- The propagation delays.

These components are discussed below.

The delay between the **L1accept** for calibration and the **Calib** signal as generated inside the **PDC** module is given by L4 minus L1 minus L3. Its value can vary from -2.2 μs (L1=15, L3=63, L4=0) to 1.4 μs (L1=0, L3=0, L4=63).

The large delay is applied to all the **L1accept** signals before the output of the **PDC** module. This delay is irrelevant in the current discussion and it will be ignored.

The re-synchronization at the input of the **PDG** module creates a delay (up to 25 ns) but no jitters. This delay is directly controlled by the delay in the **PDG** channel feeding the **PDC** module. Modifying this delay is the easiest way to adjust precisely the delay between **L1accept** and **Calib** simultaneously at the input of all the front-end cards.

The delay set in the **PDG** and **Fan-out** modules for physical triggers alignment apply to the **L1accept** signal and not to the **Calib** signal. This can add up to 220 ns to the calibration delay.

When all the delays are set to 0, the difference in processing between the **Calib** and the **L1accept** signals will induce a difference in propagation delays. This effect will be measured in the first prototype, but it is expected to be a few ns.