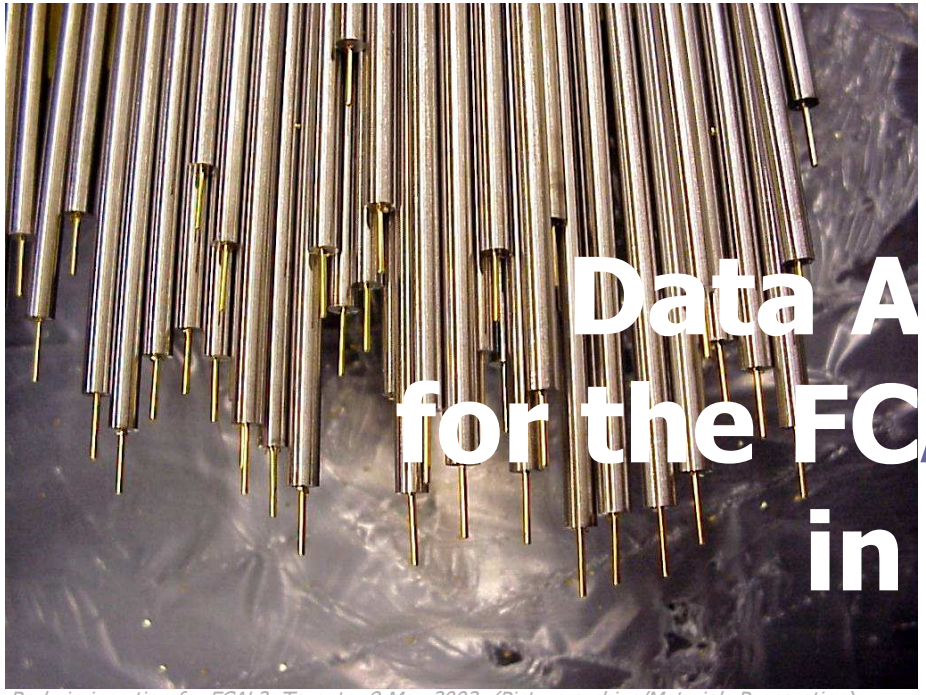


Rod pin insertion for FCAL2, Toronto, 9 May 2002 (Picture archive/Materials Preparation)

Petr Gorbounov
FCAL meeting, CERN 28 January 2003

Data Acquisition for the FCAL Beam Test in 2003

- DAQ tasks & requirements
- Review of the r/o electronics (incl. miniRODs)
- Features of existing EM and HEC DAQs
- Proposed FCAL DAQ structure
- Needs, schedule, responsibilities

DAQ tasks

core

- Calorimeter r/o , using miniRODs
- TB equipment r/o (BC, counters …)
- Electronic calibration tasks
- Configuration tasks

framework

- Run & setting control, book-keeping
- Interface with Slow Control(s)
- Data storage/archiving
- Event dislay, default online monitoring

utility

- Testing, standalone calibration tasks, eLogbook

Requirements for FCAL

- Event rate: up to ~1000 ev / spill
- Data volume: 8 FEBs -> ~1000 channels
  5-7 samples × 16 bits -> ~15 kB/event
  up to 15 MB/spill -> 60 MB/min

40 GB/day
1 TB overall

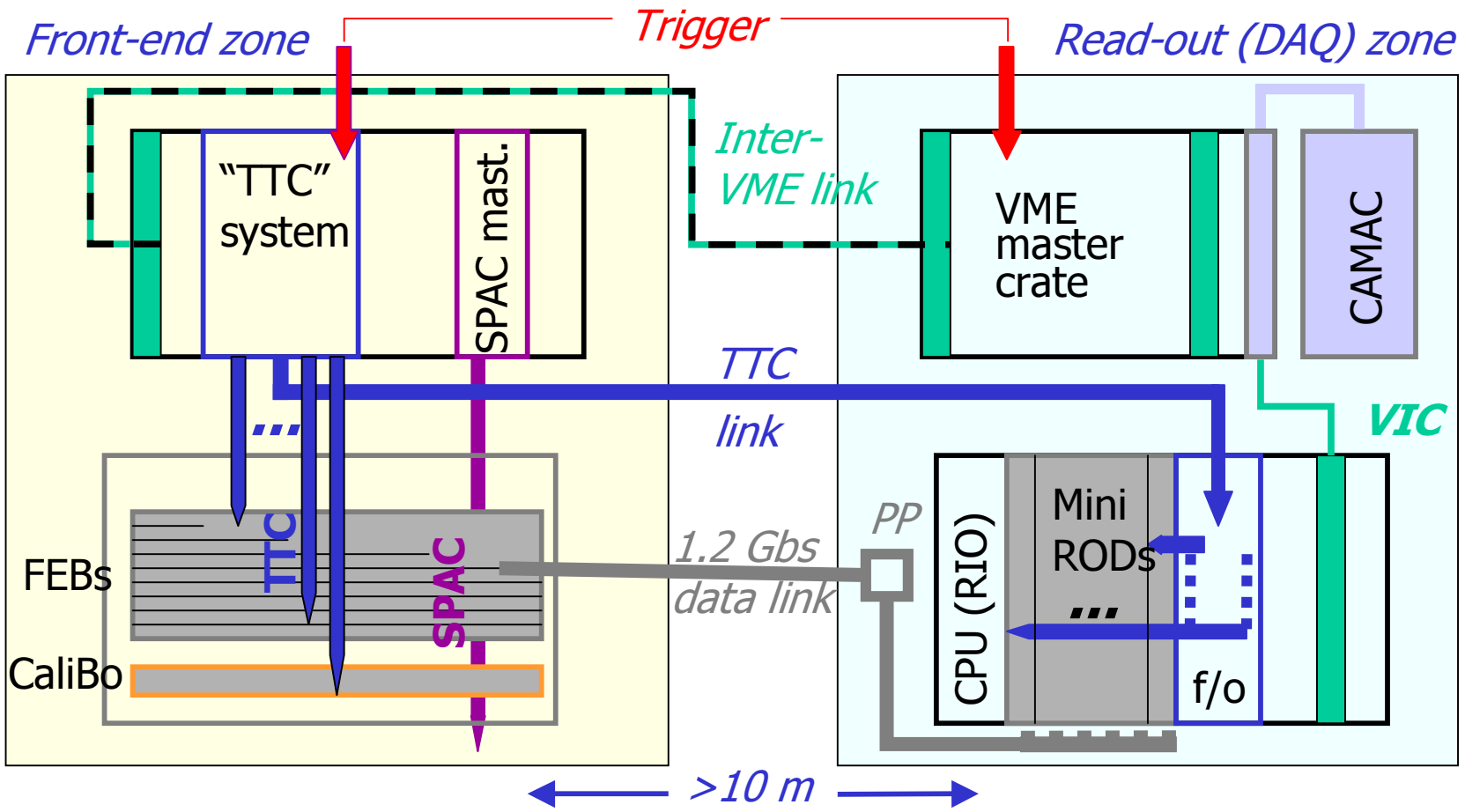
- Calibration runs (pedestals, gains, …):
  - easy to switch phys <-> calib
  - easy to configure (up to 32 samples, delay adj.)
- Buses: VIC, PCI-VME, SPAC, CAMAC, Ethernet
- Triggers: beam, calib (calo, TB), random, …
- Stable TTC and SPAC set-up
- Slow controls: HV, SPS, H6 magnets, cryogenics, FEB temperature, calo position ...

Requirements (less FCAL-specific)

- User interface
  - r/o configuration (calo, camac, BCs, TTC crate …)
  - with/without recording
  - run type, beam settings
  - predefined configurations for principal components (TTC, FEB, trigger … = config. management)
- Online monitoring
  - distributed, decoupled from DAQ
  - based on common (FORTRAN or C) s/w templates
  - use familiar histogramming package (PAW, ROOT)
- Documentation, user guides

Review of the read-out electronics

HEC and EM were using *prototype* elctronics: proto-TTC (mod-0), copper FEB-(mini)ROD link, proto-ROD (HEC) or mini-ROD (EM)

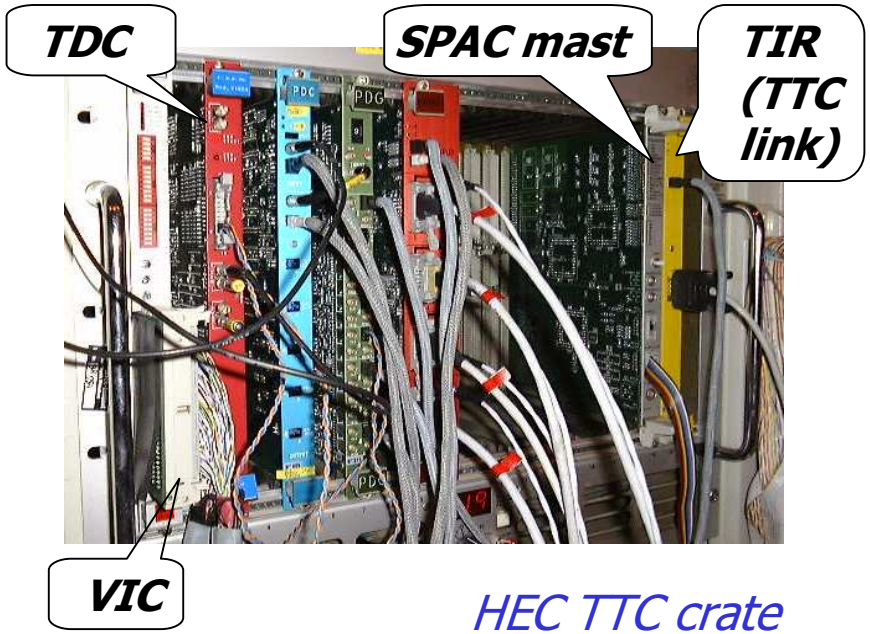


(synopsis)

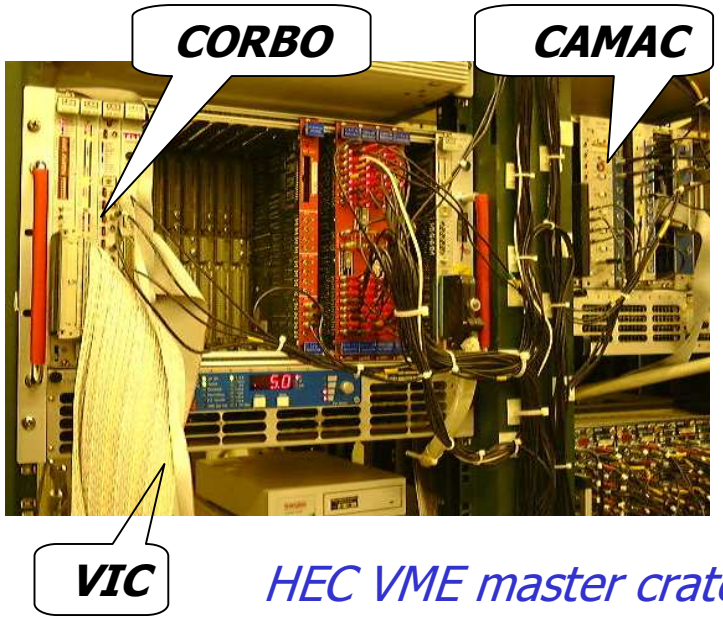
- FEB
  - preamps, shapers -> L1 sums
  - 2.5 μs (3.6 μs) analog pipelines
  - 16 × 8 ch ADCs (5 MHz, 12 bit)
  - data link driver (a full event in 9.5 μs)

  Configured via SPAC bus

  Driven by TTC signals
- Module-0 "TTC" system
  - VME modules: PDC, PDG, Fan-out(s), TIR
  - 40 MHz clock, trigger re-sync and programmable delay
  - fast signal fan-out to FEBs and miniRODs
  - TTC signals: CLK, BCR, Trig, Init, TestPulse
- SPAC
  - dedicated serial bus to download programs and config. To FEB and Cal. Boards. SPAC master: a VME module
- VIC is a VME Interconnection bus, driven by (e.g.) VIC 8251

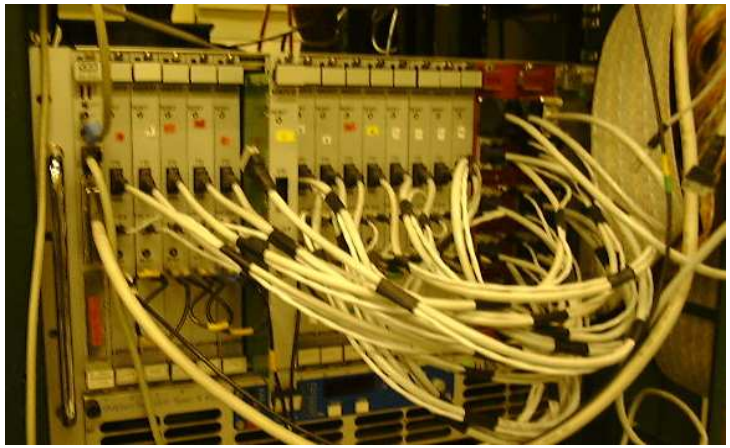


HEC TTC crate



HEC VME master crate

HEC Front-End Crate



EMb miniROD crate

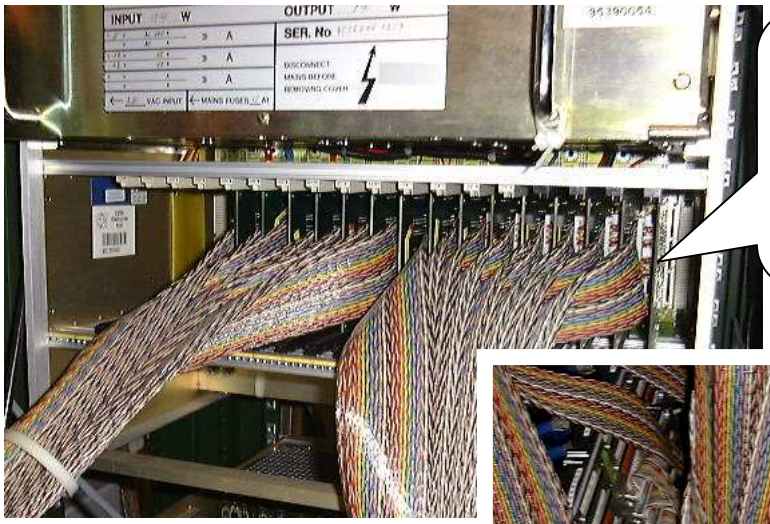
miniROD

- a VME module + link cable adapter
- one miniROD read one FEB, via a sync. 32 bit/ 40 MHz link
- 16 dual-port memories (FIFOs, one/ADC), up to 1 k ev deep (?)
- 16 bits (12: data, 2: gain, bit14: 0, bit15: bit odd parity)
- requires TTC (clk, trig, reset) for synchronization
- fully confugurable via VME
- VME port: async access to FIFOs

- TTL busy on front panel (set when FIFO is ~full)
- Test mode available (all inputs from VME)
- documentation and r/o software: available (EM, BNL)

miniROD crate and the data link

TTC fanouts



link cable adapters on the backplane

Patch Panels

EM cal DAQ (s/w, h/w)

P.Perrodo et al. (LAPP Annecy): *"…This s/w is designed to be used by anyone who wants to work with it…"*

- Good documentation, Atlas Note ATC-TT-EN-002
- Online and low-level offline codes: available
- miniROD configuration and r/o: a standalone C-program **MRA** free-running on RIO 8062 CPU. DAQ reads the RIO buffer at end-of-burst.
- Main DAQ: based on RD13 DAQ/EF-1; running on a RAID CPU (VME board); CAMAC: via CBD 8210
- VME crates communicate via VIC (8250, 8251), except the TTC crate (via SPAC link and SVCC)
- CDR, monitoring: HP w/station with a built-in VME

We can use: miniROD crate (RIO?), MRA

RIO 8062

HEC DAQ (s/w, h/w)

Author: K. (Sepp) Hubert (MPI)

- Proprietary text-menu driven run/configuration control
- Codes: available, with some documentation
- Main DAQ: runs on a RAID CPU
- VME crates communicate via VIC 8251, including the TTC crate (possible ground loop problems??)
- CAMAC: via CBD 8210; CDR / monitoring: HP
- Trigger input to DAQ: via VME CORBO (RBD 8047)
- Prototype ROD boards for the FEB r/o

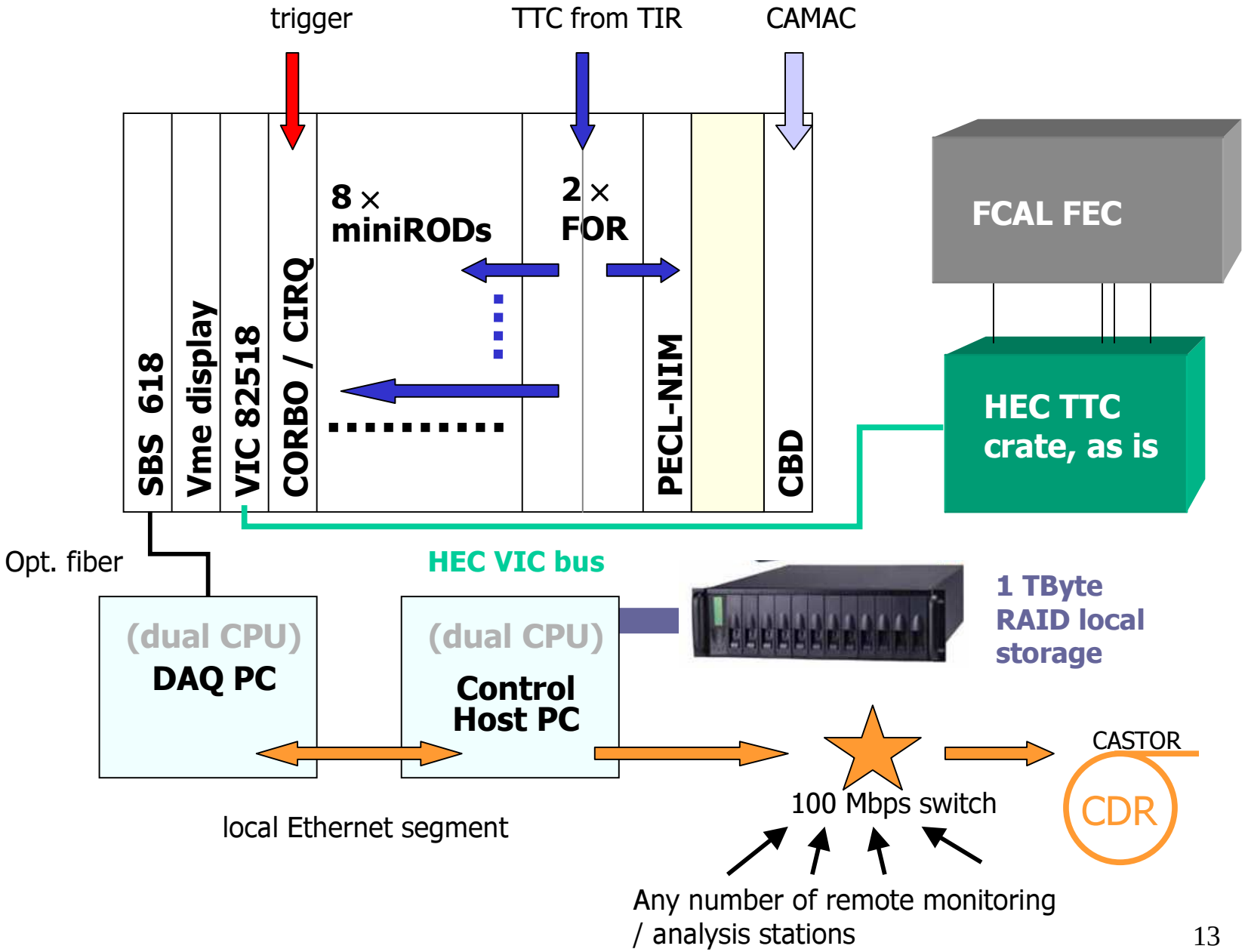
CORBO

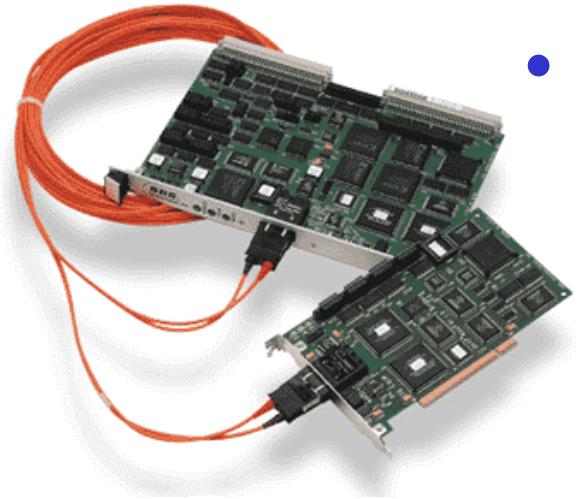
We could use: HEC VIC-mapping, the TTC crate and its s/w, the (EPIO compatible) raw data format

Proposed FCAL DAQ structure

- max. use of the existing core software from EM and HEC
- if possible, use the HEC and EMEC DAQ infrastructure (HEC counting room, FEB-ROD cables, Ethernet connections, HEC TTC crate with its VIC link to the CR)
- replace a "zoo" of obsolete CPUs (RIO, RAID, HP) with a single host scheme based on a (dual-CPU) Linux-based PC and a 32 MB/s PCI-VME interface SBS 618 ("bit3")

  ⇨ profit from PCI system resources (CPU, memory, OS, application software, peripherals)
- single VME crate at the DAQ side + a CAMAC crate
- use a mature, well-tested generic DAQ framework
  - **MIDAS** (TRIUMF, PSI) … was used by ITEP for BPC tests
  - **DATE** (ALICE) … used by COMPASS, HARP and ALICE TBs
- use Central Data Recording (CDR) and a local backup


trigger
TTC from TIR
CAMAC
8 × miniRODs
2 × FOR
SBS 618
Vme display
VIC 82518
CORBO / CIRQ
PECL-NIM
CBD
FCAL FEC
HEC TTC crate, as is
Opt. fiber
HEC VIC bus
(dual CPU) DAQ PC
(dual CPU) Control Host PC
1 TByte RAID local storage
CASTOR
CDR
100 Mbps switch
local Ethernet segment
Any number of remote monitoring / analysis stations

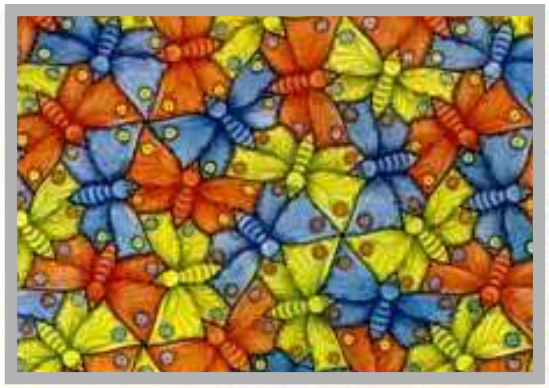


- SBS 618 ("bit3") PCI-VMI interface
  - popular at CERN, we have one (borrowed from INFN)
  - commercial LINUX driver is available
  - some experience with Lar r/o (@ BNL)
  - DME transfers: up to 32 MB/s

- Other VME units (except CORBO): available from EP Pool
- CORBO: borrow from EM (?). Alternative: CIRQ (Harp/CHORUS)
- DAQ PCs: the proposed scheme would work even with a single standard desktop PC. Scalability: -> industrial PC -> Control Host PC -> RAID storage
- Redundant Array of Inexpensive Disks: allows one HDD w/o impact on the integrity of data. Automatic disk rebuild (hot global spare HDD, hot swappable HDDs (?)

Questions, needs

- Decision on the FEC (construct new one, refurbish the EM or HEC crate?)
- Doc. on the FEB. Is the module-0 TTC system compatible with it? Same for the Calibr. Board. Who's TTC crate do we take?
- Detailed description of the electronic calibration procedures?
- Channel mapping for the 2003 tests?
- Decision on the counting room, location of electronics and DAQ racks. Dates? (given that the HEC cold tests are ongoing)
- Allocation of FEB-ROD cables ?



- DAQ-specific h/w needs
  - dedicated PCs, RAID storage system: buy or not?
  - one more "bit3" with a >10 m opto-cable; a UPS for the RAID

(*) M.C. Escher "Symmetry E70, Butterflies". 1948

(my) Schedule

- February (3 weeks)
  - low-level tests in the lab with "bit3", CAMAC, VME/VIC mapping
  - standalone miniROD r/o tests
  - evaluation of DAQ framework candidates, decision
- March (3.5 weeks)
  - TTC system integration, decision on the TTC crate controller
  - SPS and H6 data r/o
  - upon delivery of new PCs: tandem operation tests, networking tests
  - when FEC is available: integration tests (SPAC-CaliBo-FEB-miniROD)
- April-midMay (6 weeks)
  - installation in the H6 zone, cabling
  - calibration procedures
  - DAQ s/w consolidation; work on the online monitoring
- end-May (2 weeks)
  - installation of the BPCs, integration, tests with beam

Responsibilities (*)

- P. Gorbounov:
  - online r/o software, VME and CAMAC h/w, miniRODs, SPAC software
  - run control, "provider" part of the on-line monitoring
  - raw-data format
- …
  - online monitoring, shifter's procedures
  - configuration book-keeping (DB?)
  - data archiving, CDR
- …
  - slow controls, SPS data, H6 information
  - calibration procedures
- …
  - trigger set-up (together with PG) , timing
  - FEC, FEBs, Calibration Board
  - TTC system
- …
  - beam equipment
- …
  - cabling assistant
  - electronics assistant
- …
  - LINUX system support

(*) EM: TB support team = 14-16 people